Initially, the present specification is amended to correct a minor informality. Specifically, B_2H_6 is mentioned as an n-type impurity gas in the specification on page 7, line 31, page 10, line 14 and page 11, line 17. This portion of the specification has been amended to change "B_2H_6/SiH_4" to "PH_3/SiH_4." It is respectfully submitted that one of ordinary skill in the art would readily recognize that boron (B) is a p-type impurity and phosphorous (P) is an n-type impurity (cf. attached article "*Principles of Growth and Proceeding of Semiconductors*, page 27"). Also, phosphine gas (PH_3) is generally used as the n-type impurity gas. Thus, the forgoing amendment is believed to be proper and favorable consideration is requested.

The Official Action rejects claims 1-8 and 11-16 under 35 U.S.C. §103(a) as being unpatentable over Wakai et al. in view of Tsumura et al. The Official Action asserts that Wakai et al. disclose an inverted staggered TFT constituted by a substrate 101, a gate insulating film 103, a semiconductor layer 104, an insulating film 108 and a transparent electrode 110. Also, the Official Action asserts that Tsumura et al. discloses a substrate 1 can be made of industrial plastics such as polyimide and polyphenylene sulfide film, and a layer 3 can be made of polymers (resinous layer it is inherent).

Applicant respectfully disagrees. Specifically, Applicant traverses the assertion that layer 3 of Tsumura et al. is inherently a resinous layer. In the case of Tsumura et al., the layer 3does not function as the claimed resinous layer but as a gate insulating film (column 3, lines 50-61). The essence of the present invention is that the resinous layer is formed on an uneven surface of a resinous substrate in order to planarize the base on which the semiconductor device is formed (Specification, page 6, lines 25-29). Furthermore, the present invention clearly teaches a resinous substrate 101, the resinous layer 102, and the gate insulating film 104, respectively (Figure 1). That is, the present application discloses and claims both a resinous layer and a gate insulating film. Tsumura et al. never disclose or suggest the structure and the purpose of the present invention and thus it is respectfully submitted that one of skill in the art would not have been motivated to combine or modify Wakai and Tsumura as asserted in the Official Action. It is respectfully submitted that the

B

above remarks are applicable to Figure 7 of Tsumura et al. Reconsideration is requested in view of the above.

Also, with respect to claims 1-3 rejected under 35 U.S.C §103(a) as being unpatentable over Wakai et al. in view of Koezuka et al., the Official Action asserts that Koezuka et al. discloses a substrate 1 can be made of polysilicon and an insulating layer 3 can be polyethylene (resinous layer). However, similarly to Tsumura et al., the insulating layer 3 of Koezuka et al. does not function as the resinous film for planarizing the base on which the semiconductor device is formed, but as a gate insulating film. Therefore, Applicant believes that the rejection is not appropriate and requests reconsideration in view of the above.

For all of the above reasons, it is respectively asserted that claims 1-8 and 11-37 are now in proper condition for allowance. Reconsideration of these claims in view of the above comments is respectively requested. If the Examiner feels that any further discussions would be beneficial in this matter, it is requested that the undersigned be contacted.

Respectfully submitted,

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